12-V, 3-PHASE, SENSORLESS BLDC MOTOR DRIVER

Check for Samples: DRV11873

FEATURES

- **Input Voltage Range 5 V to 16 V**
- **Six Integrated MOSFETs With 1.5-A Continuous Output Current**
- **Total Driver H+L R_{DSON} 450 mΩ**
- **Sensorless Proprietary BMEF Control Scheme**
- **150° Commutation**
- **Synchronous Rectification PWM Operation**
- **FG and RD Open Drain Output**
- **5-V LDO for External Use**
- **PWM_{IN} Input From 15 kHz to 100 kHz**
- **Over Current Protection With Adjustable Limit Through External Resistor**
- **Lock Detection**
- **Voltage Surge Protection**
- **UVLO**
- **Thermal Shutdown**

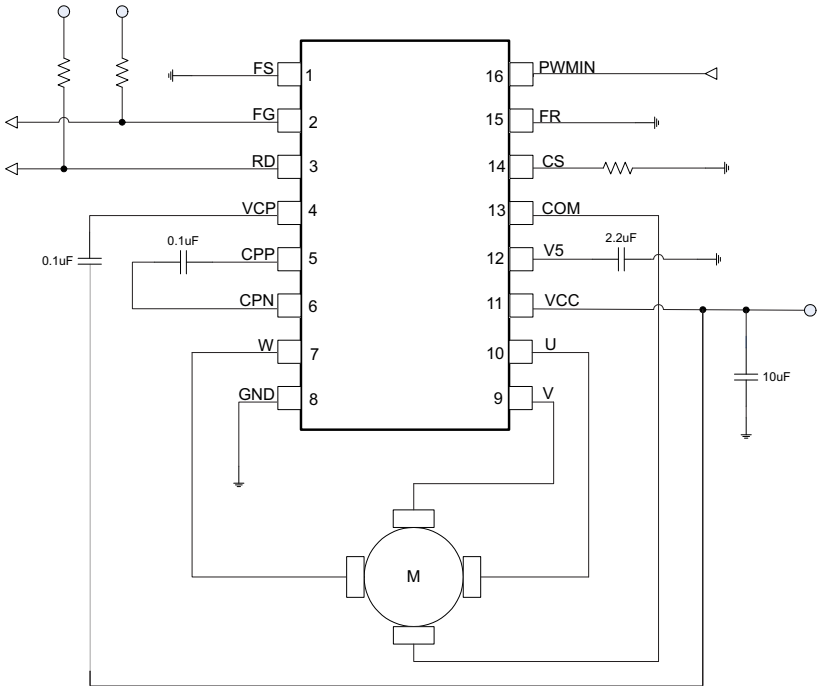
APPLICATIONS

- **Appliance Cooling Fan**
- **Desktop Cooling Fan**
- **Server Cooling Fan**

DESCRIPTION

DRV11873 is a three phase, sensorless motor driver with integrated power MOSFETs with drive current capability up to 1.5-A continuous and 2-A peak. DRV11873 is specifically designed for low noise and low external component count fan motor drive applications. DRV11873 has built in over current protection with no external current sense resistor needed. The synchronous rectification mode of operation achieves increased efficiency for motor driver applications. DRV11873 outputs FG and RD to indicate motor status with open drain output. A 150° sensorless BEMF control scheme is implemented for a three phase motor. DRV11873 is available in the thermally efficient 16-pin TSSOP package. The operation temperature is specified from -40°C to 125°C.

TYPICAL APPLICATION



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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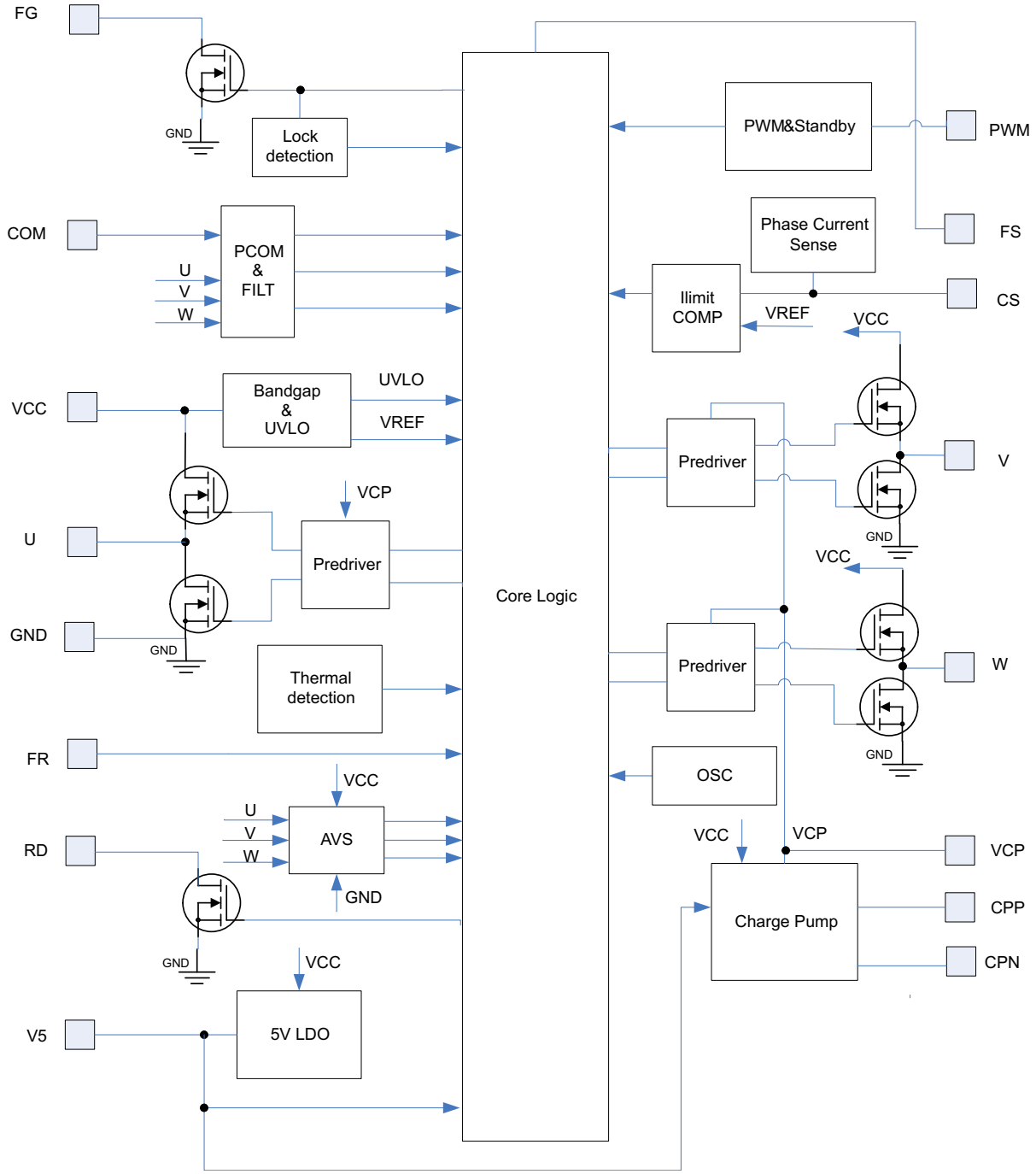
ORDERING INFORMATION(1)

T_A	PACKAGE(2)		PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP-16 (PWP)	Tape and reel, 3000	DRV11873PWP	11873

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.

FUNCTIONAL BLOCK DIAGRAM



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PIN DESIGNATION

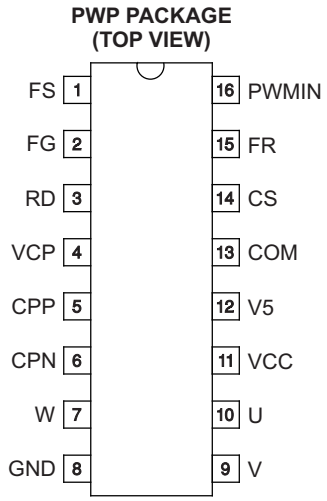

Table 1. PIN DESCRIPTIONS

TERMINAL		I/O (1)	DESCRIPTION
NAME	NO.		
FS	1	I	Motor parameter adjustment pin. Pull low for lower speed motor and pull high for high speed motor.
FG	2	O	Frequency generator output. The output have period equal to 6 electrical states (FG).
RD	3	O	In the lock condition, RD output high through a pull up resistor to V_{CC} or 5 V.
VCP	4	O	Charge pump output
CPP	5	O	Charge pump conversion terminal
CPN	6	O	Charge pump conversion terminal
W	7	O	Phase W output
GND	8	-	Ground pin
V	9	O	Phase V output
U	10	O	Phase U output
VCC	11	I	Input voltage for motor and chip supply voltage
V5	12	O	5-V regulator output
COM	13	I	Motor common terminal input
CS	14	I	Over current threshold set up pin. A resistor set up current limit is connected between this pin and ground. The voltage across the resistor will compare with the voltage converted from the bottom MOSFETs current. If MOSFETs current is high, the part will get into the over-current protection mode by turning off top PWM MOSFET and keeping the bottom MOSFET on. $I_{limit}(A) = 6600/R_{CS}(\Omega)$, Equation valid range: 500 mA < I_{limit} < 2000 mA
FR	15	I	Set high for reverse rotation. Set low or floating for forward rotation.
PWMIN	16	I	PWM input pin. The PWM input signal will be converted to a fixed switching frequency on MOSFET driver. The PWM input signal resolution is less than 1%.

(1) I = input, O = output, N/A = not available

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VCC	-0.3	20	V
	CS	-0.3	3.6	
	PWMIN, FS, FR	-0.3	6	
	GND	-0.3	0.3	
	COM	-1	20	
Output voltage range	U, V, W	-1	20	V
	FG, RD	-0.3	20	
	VCP	-0.3	25	
	CPN	-0.3	20	
	CPP	-0.3	25	
	V5	-0.3	6	
Electrostatic discharge (ESD)	Human body model, HBM		4	kV
	Charge device model, CBM		1	
	Machine model, MM		200	V
T_J Operating junction temperature		-40	125	°C
T_{stg} Storage temperature		-55	150	°C

THERMAL INFORMATION

THERMAL METRIC[1]		DRV11873 PWP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	39.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	30.3	
θ_{JB}	Junction-to-board thermal resistance[4]	25.6	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.5	
ψ_{JB}	Junction-to-board characterization parameter[6]	10.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	3.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VCC	5	16	V
Voltage range	U, V, W	-0.7	17	V
	COM	-0.1	17	
	FG, RD	-0.1	16	
	PGND, GND	-0.1	0.1	
	VCP	-0.1	22	
	CPP	-0.1	22	
	CPN	-0.1	16	
	V5	-0.1	5.5	
	PWMIN, FR, FS	-0.1	5.5	
Operating junction temperature, T_J		-40	125	V

ELECTRICAL CHARACTERISTICS

Supply Current

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VCC}	Supply current	T_A = 25°C; PWM = V_{CC}; V_{CC} = 12 V		2.7	5	mA

UVLO

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VUVLO-th_r}$	UVLO threshold voltage	Rise threshold, T_A = 25°C		4.3	4.6	V
$V_{UVLO-th_f}$	UVLO threshold voltage	Fall threshold, T_A = 25°C	3.9	4.1		V
$V_{UVLO-thhys}$	UVLO threshold voltage hysteresis	T_A = 25°C	100	200	300	mV

Integrated MOSFET

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON}	Series resistance(H+L)	T_A = 25°C; V_{CC} = 12 V; VCP = 19 V; I_{OUT} = 1.5 A		0.45	0.6	Ω

PWM

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PWM-IH}	High-level input voltage	V_{CC} ≥ 4.5 V	2.7			V
V_{PWM-IL}	Low-level input voltage	V_{CC} ≥ 4.5 V			0.8	V
f_{PWM}	PWM input frequency		15		100	kHz
$I_{PWM-SOURCE}$	PWM source current		35	50	65	µA

FG

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{FG-SINK}$	FG pin sink current	V_{FG} = 0.3 V	5			mA
$I_{FG-short}$	FG pin short current limit	V_{FG} = 12 V		20	25	mA

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RD

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{RD\text{-}SINK}$	RD pin sink current	V_{RD} = 0.3 V	5			mA
$I_{RD\text{-}short}$	RD pin short current limit	V_{RD} = 12 V		20	25	mA

FR and FS

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FR\text{-}IH}$	High-level input voltage	V_{CC} ≥ 4.5 V	2.3			V
$V_{FR\text{-}IL}$	Low-level input voltage	V_{CC} ≥ 4.5 V			0.8	V
$V_{FS\text{-}th}$	FS set threshold voltage	V_{CC} ≥ 4.5 V	2.3		0.8	V

V5

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V5	5V LDO voltage	V_{CC} = 12 V	4.75	5	5.25	V
I_{V5}	5V LDO load current	V_{CC} = 12 V		20		mA

Lock Protection

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{LOCK\text{-}ON}$	Lock detect time	FS = 0	0.875	1.25	1.625	s
		FS = 1	0.437	0.625	0.812	
$T_{LOCK\text{-}OFF}$	Lock release time	FS = 0	4.375	6.25	8.125	s
		FS = 1	2.187	3.125	4.06	

Current Limit

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current limit	CS pin to GND resistor = 3.3 kΩ	1.7	2	2.3	A

Thermal Shutdown

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SDN}	Shut down temperature threshold	Shut down temperature		160		°C
		Hysteresis		10		

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DETAILED DEVICE DESCRIPTION

DRV11873 is a three phase, sensorless motor driver with integrated power MOSFETs with drive current capability up to 1.5-A continuous and 2-A peak. It is specifically designed for low noise and low external component count fan motor drive applications. DRV11873 has built in over current protection with no external current sense resistor needed. The synchronous rectification mode of operation achieves increased efficiency for motor driver applications. DRV11873 outputs FG and RD to indicate motor status with open drain output. A 150° sensorless BEMF control scheme was implemented for a three phase motor. DRV11873 can fit a wide range of fan motors with the FS pin selection function. Voltage surge protection scheme prevents the input V_{CC} capacitor from over charge during motor braking mode. DRV11873 has multiple built in protection blocks including UVLO, over current protection, lock protection and thermal shut down protection.

SPEED CONTROL

DRV11873 can control motor speed through either the PWM_{IN} or V_{CC} pin. Motor speed will increase with higher PWM_{IN} duty cycle or V_{CC} input voltage. The curve of motor speed (RPM) vs PWM_{IN} duty cycle or V_{CC} input voltage is close to linear in most cases. However, motor characteristics will affect the linearity of this speed curve. DRV11873 can operate at low V_{CC} input voltage down to 4.1 V. The PWM_{IN} pin is pulled up to V5 internally and the frequency range can vary from 15 kHz to 100 kHz. The motor driver MOSFETs will operate at constant switching frequency 125 kHz when the FS pin is pulled high and 62.5 kHz when the FS pin is pulled low. With this high switching frequency, DRV11873 can eliminate audible noise and reduce the ripple of V_{CC} input voltage and current.

FREQUENCY GENERATOR

FG output is a 50% duty square wave output in the normal operation condition. Its frequency represents the motor speed and phase information. FG pin is an open drian output. An external pull up resistor is needed to connect external system. During the start up FG output will stay at high impedance until the motor speed reaches certain level and BEMF is detected. If FG is not used, this pin can be left for floating. FG pin can be tie to either 5 V or V_{CC} through a pull up resistor. Normally the pull up resistor value can be 100 kΩ or higher. During lock protection condition, FG output will keep high until the lockout protection is dismissed and restart completed. A current limit function has been built in for FG pin. It will prevent FG open drain MOSFET get damaged in case V_{CC} or 5 V directly connected to FG pin by accident. To calculate RPM based on FG frequency, please refer to below equation.

$$\text{RPM} = \frac{(\text{FG} \times 60)}{\text{pole pairs}} \tag{1}$$

Where FG is in hertz (Hz).

FS SETTING

DRV11873 can fit a wide range of fan motors by setting the FS pin. For high speed fan motors with low motor winding resistance and low inductance, the FS pin should be pulled high. For low speed fan motors with high motor winding resistance and high inductance, the FS pin should be pulled low. Through FS pin selection, DRV11873 can be used for wide applications from low speed refrigerator cooling fans to high speed server cooling fans. FS status can only be set during device power up.

LOCK PROTECTION AND RD OUTPUT

If the motor is blocked or stopped by the external force, the lock protection will be triggered after detection time. During lock detection time, the circuit monitors FG signal. If the FG output is high during lock detection time, the lock protection will stop driving the motor. After lock release time, DRV11873 will resume driving the motor. If the lock condition is still there, DRV11873 will proceed with next lock protection cycle until the lock condition is removed. With this lock protection, the motor and device will not get over heated or be damaged. A different FS setting will determine a different lock detection and lock release time.

The RD pin is an open drain output which can be tied to either V5 or V_{CC} through a pull-up resistor. Normally the pull-up resistor value can be 100 kΩ or higher. During the lock protection condition, RD output will keep high until the lock protection is dismissed and restart completed. A current limit function has been built in for the RD pin which prevents the open drain MOSFET from damage in case V_{CC} or V5 directly connects to the RD pin.

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REVERSE SPIN CONTROL FR

DRV11873 has an FR pin to set the motor for a forward spin or reverse spin. During DRV11873 power up, FR status will be set. During normal operation, the spin direction of the motor will not be changed when the FR status is changed. The FR status can be reset after the next PWM rising edge if PWM_{IN} was pulled low for 300 µs (when the FS status is high) or 600 µs (when the FS status is low).

5-V LDO

DRV11873 has a built-in 5-V LDO which can output a 20-mA load current. It can provide 5-V bias voltage for external use. A 2.2-µF ceramic capacitor is recommend to connect closely on the PCB layout between V-5 pin and ground.

OVER CURRENT PROTECTION

DRV11873 can adjust over current point through the external resistor connected to CS pin and ground. Without using external current sense resistor, DRV11873 senses the current through power MOSFET. Therefore there is no power loss during the current sensing. This current sense architecture improves the system efficiency. Short CS pin to ground will disable over current protection. During over current protection, DRV11873 will only limit the current to the motor and it will not shut down the operation. The over current threshold can be set by the value of current sensing resistor through Equation 2.

$$I\,(A) = \frac{6600}{R_{CS}\,(\Omega)} \tag{2}$$

UVLO

DRV11873 has a built-in UVLO function block. The hysteresis of UVLO threshold is 200 mV. The device will be locked out when V_{CC} reaches 4.1 V and woke up at 4.3 V.

THERMAL SHUTDOWN

DRV11873 has a built in thermal shunt down function, which will shut down the device when the junction temperature is over 160°C and will resume operating when the junction temperature drops back to 150°C.

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APPLICATION INFORMATION

DRV11873 only requires 5 external components. A 10-µF or higher ceramic capacitor connected to V_{CC} and ground is needed for decoupling purpose. During layout, the strategy of ground copper pour is very important to enhance the thermal performance. For two or more layers, eight thermal vias are needed. Refer to Figure 1 for an example of PCB layout. For high speed motors (FS = 1), which need higher start up current, three Schottkey diodes are needed between phases U, V, W and ground. Each diode anode terminal needs to be connected to ground and cathode terminal needs to be connected to either U or V or W.

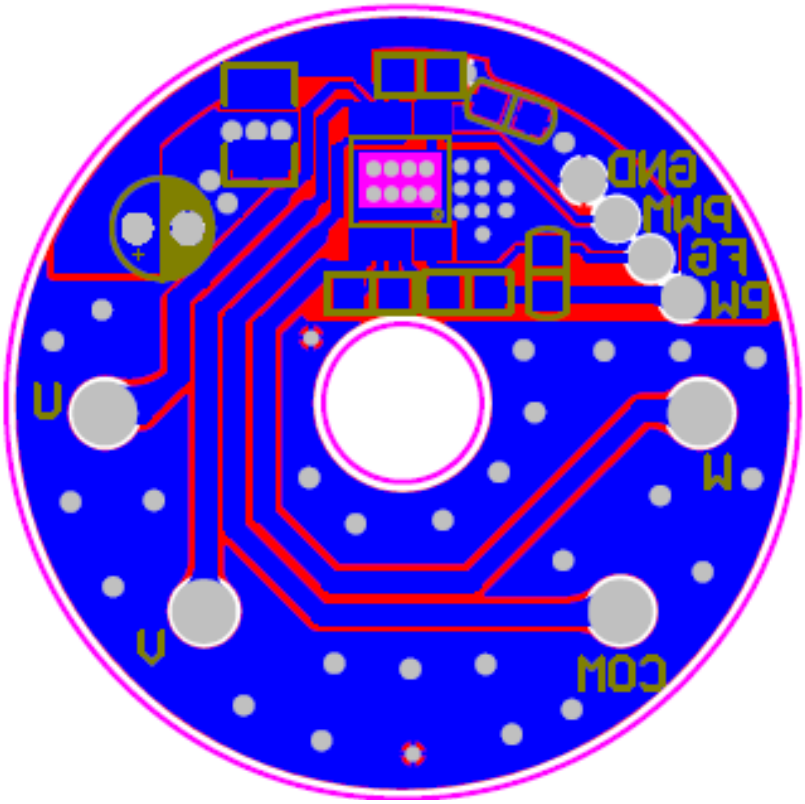

Figure 1. PCB Layout

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DRV11873PWPR	PREVIEW	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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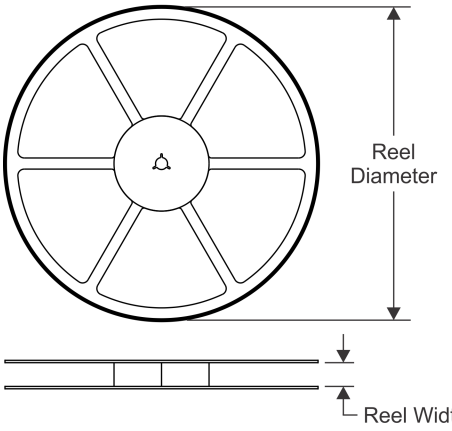
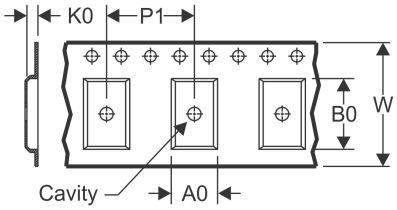
TAPE AND REEL INFORMATION

REEL DIMENSIONS

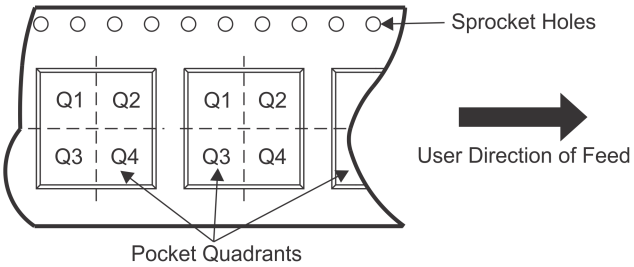


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

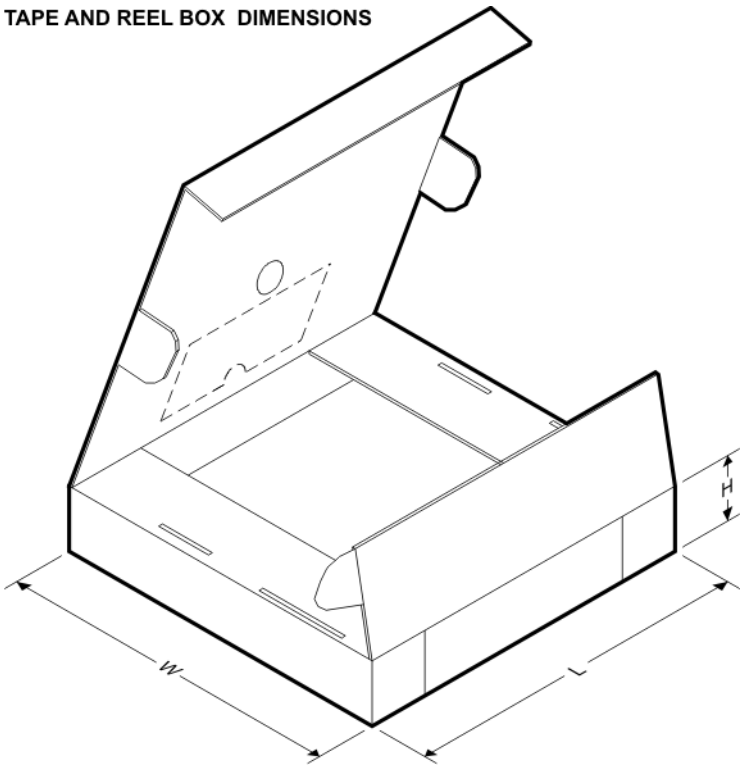
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV11873PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

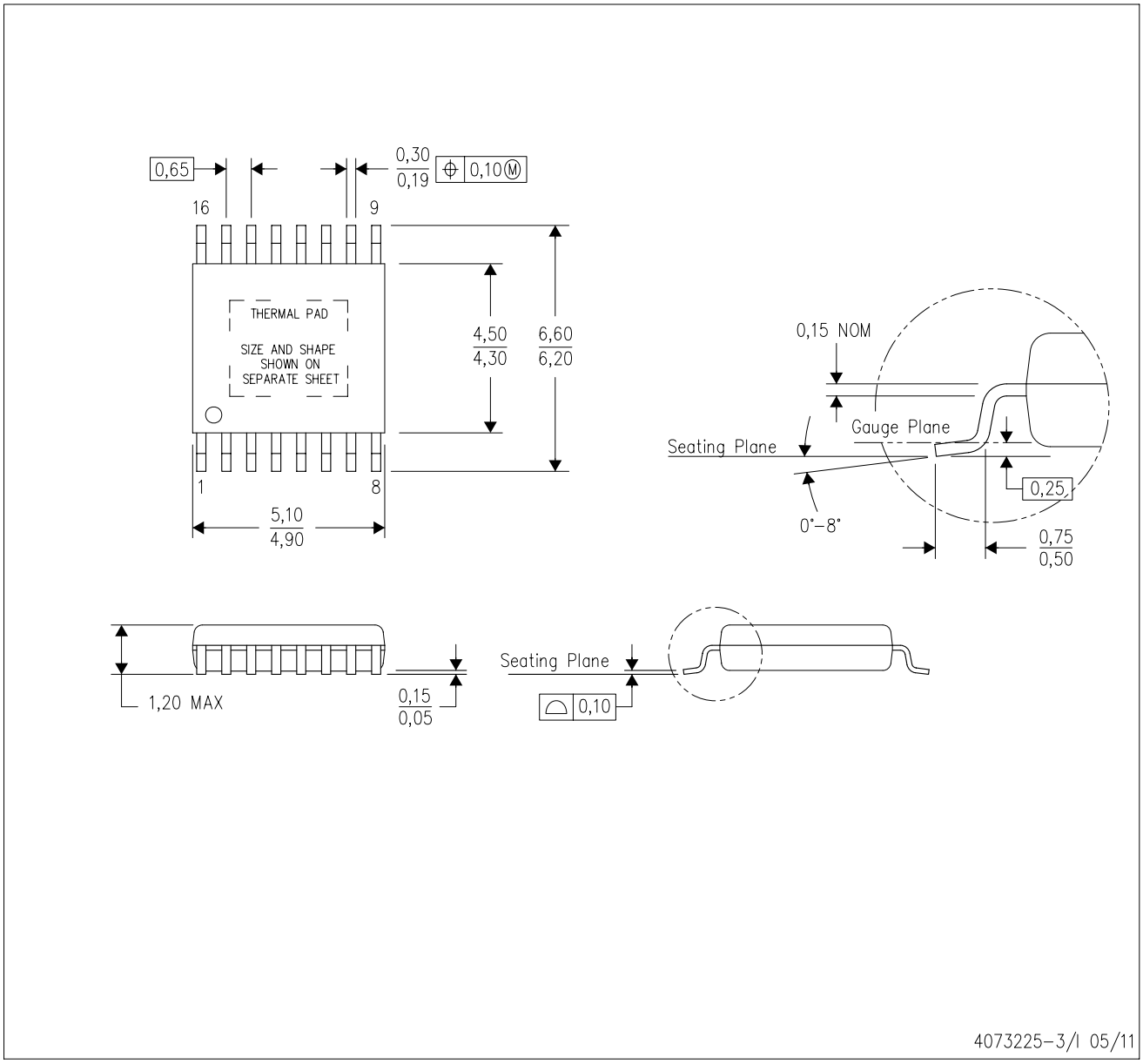
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV11873PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

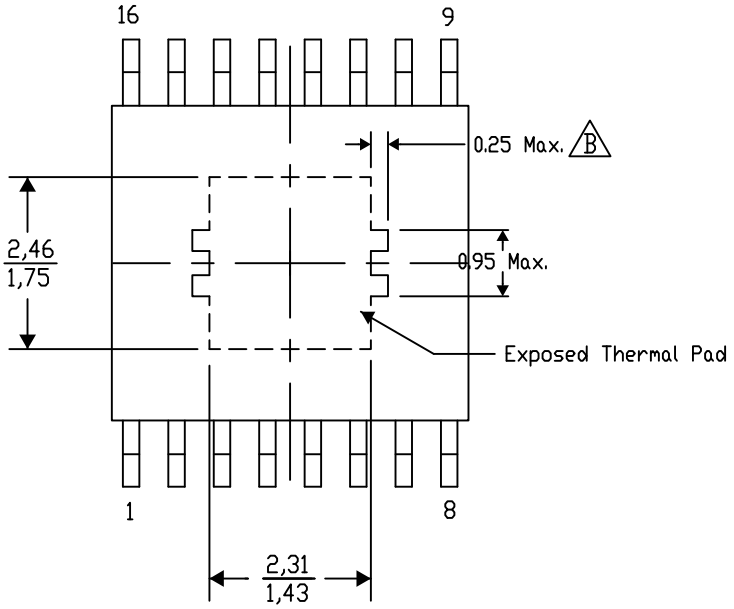
PWP (R-PDSO-G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

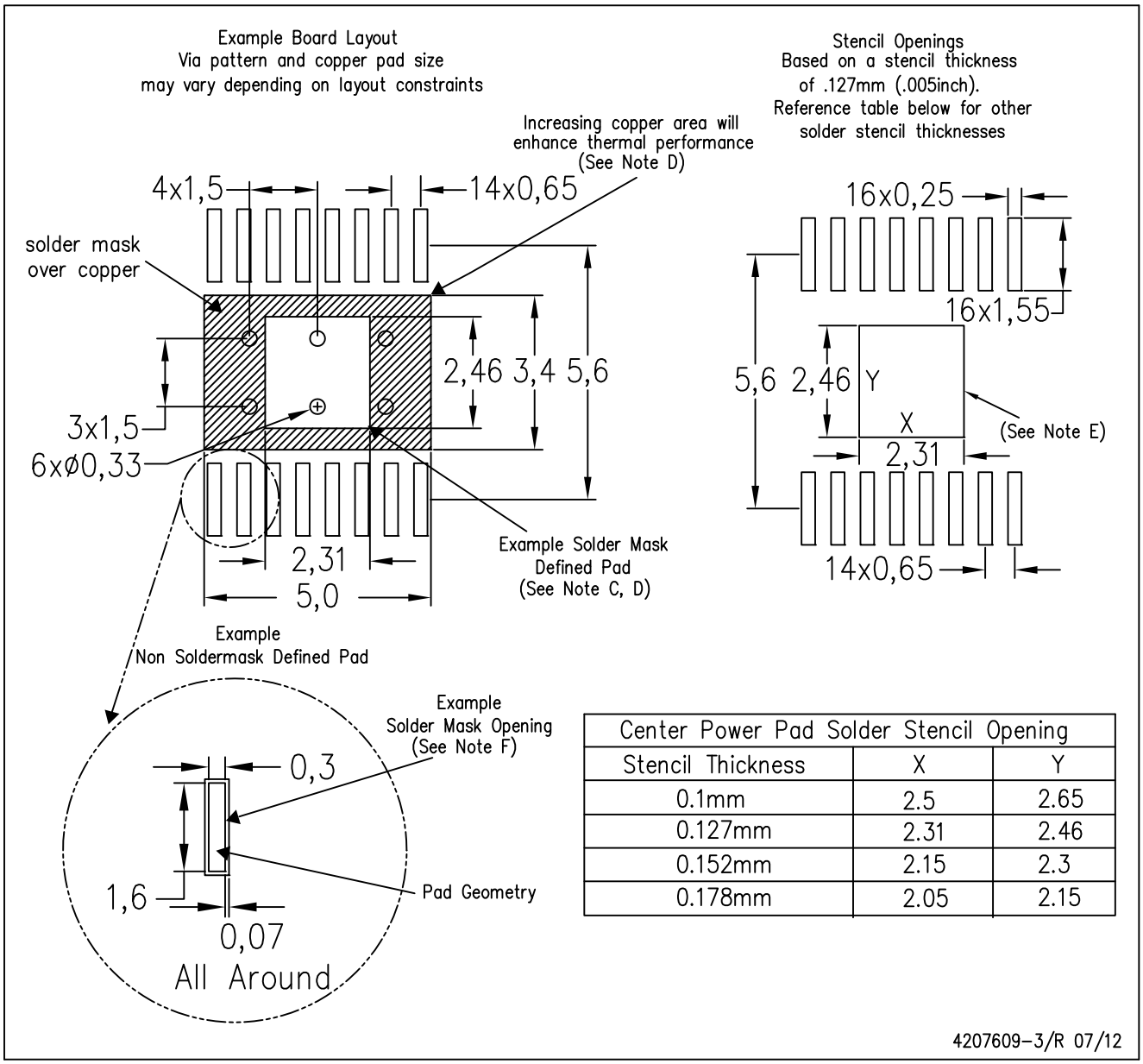
4206332-6/AC 07/12

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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